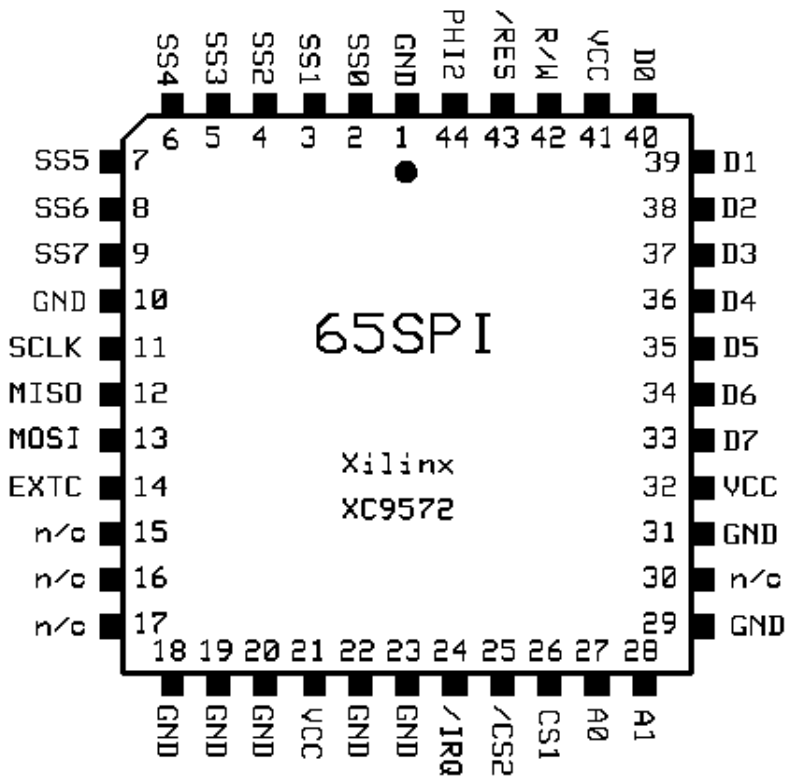
Rev 3 – June 29, 2008

65SPI

An SPI interface for the 65C02 family of microprocessors

This device was created to provide a basic SPI interface for the 65xx family of microprocessors. Currently, the only way to provide SPI is to bit-bang it using a 6522 or equivalent device. That uses a lot of microprocessor time and program space. This device takes care of the data loading, shifting, clocking, and control - freeing the microprocessor for more important duties. There is interrupt support to allow an ISR to handle the SPI interface. The status register provides signals for polling if interrupts are not desired.

Chip Layout:



44 pin PLCC

Pin Descriptions

A0-A1	Microprocessor address bus (input)
CS1	Chip select, active high (input)
/CS2	Chip select, active low (input)
D0-D7	Microprocessor data bus (bidirectional)
EXTC	External shift clock (optional input)
GND	System ground
/IRQ	Microprocessor interrupt line, active low (output)
MISO	SPI Master In, Slave Out line (input)
MOSI	SPI Master Out, Slave In line (output)
PHI2	Microprocessor system clock (input)
/RES	Microprocessor reset line, active low (input)
R/W	Microprocessor data read/write line (input)
SCLK	SPI Shift Clock output
SS0-SS7	Slave Select lines (outputs)
VCC	System +5vdc
n/c	No connection

Features:

- CPU bus is compatible with 65C02 and 65C816 microprocessors
- Uses 4-byte memory map for host access to registers
- Operates as an SPI master
- SCLK derived from PHI2 or an External Clock source
- SCLK has an 6 bit programmable divider – CLK/2 through CLK/128
- SPI Mode 0, 1, 2, 3 supported
- Shifts MSB first
- 8-bit Slave select register with 8 Slave Select outputs
- External slave select decoding can yield up to 255 addresses.
- Direct slave select decoding yields 8 devices
- Programmable interrupt
- Interrupt or polled transmit complete flags

Register Address Map

CS1	/CS2	PHI2	A1	A0	R/W=1 (Read)	R/W=0 (Write)
0	x	x	x	x	Hi-Z	Hi-Z
x	1	x	x	x	Hi-Z	Hi-Z
x	x	0	x	x	Hi-Z	Hi-Z
1	0	1	0	0	SPI Data In	SPI Data Out
1	0	1	0	1	SPI Status	SPI Control
1	0	1	1	0	SCLK Divisor	SCLK Divisor
1	0	1	1	1	Slave Select	Slave Select

x = don't care

Register Descriptions

SPI Data

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(read/write)

The SPI Data register contains data to be shifted in/out to the slave devices. Reading the register will also clear the internal Transmission Completed flag and clear the external IRQ line, if enabled. Writing this register will start a shifting sequence. The transmit and receive data registers are single buffered. The receive buffer must be read before writing another byte to prevent incoming data loss. If you write a byte while shifting is in progress, the previous byte will become corrupted and the new byte will not be shifted.

SPI Status

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC	IER	BSY	FRX	TMO	ECE	CPOL	CPHA

(read only)

The SPI Status register provides status of the following internal flags:

TC Transmission Complete – This flag is set when the last bit has been shifted and is cleared when the SPI Data register is read.

IER Interrupt Enable – Interrupts are enabled when this is set to 1 and disabled when set to 0.

BSY SPI Busy – This is 1 when data is written to the SPI data register and will stay high until the last bit is shifted.

FRX Fast Receive mode – When set to 1, fast receive mode triggers shifting upon reading or writing the SPI Data register. When set to 0, shifting is only triggered by writing the SPI data register.

TMO Tri-state MOSI - When set to 1, the MOSI pin will be tri-stated. When set to 0, the MOSI pin will have an active output. Tri-state will allow some three-wire interfaces to work properly.

ECE External Clock Enable – This flag displays the selected shift clock source. 0 = PHI2 and 1 = external Shift clock pin (14).

CPOL Clock Polarity – This flag displays the shift clock polarity.
0 = Rising edge; 1 = Falling edge

CPHA Clock Phase – This flag displays the shift clock phase.
0 = Leading edge; 1 = Trailing edge

SPI Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	IER		FRX	TMO	ECE	CPOL	CPHA

(write only)

The SPI Control register is used to select operating conditions within the SPI controller. All bits are set to 0 on power up and when /RES is low.

IER Interrupt Enable – This bit sets the interrupt enable flag
1= interrupts enabled and 0 = interrupts disabled.

FRX Fast Receive mode – When set to 1, fast receive mode triggers shifting upon reading or writing the SPI Data register. When set to 0, shifting is only triggered by writing the SPI data register.

TMO Tri-state MOSI - When set to 1, the MOSI pin will be tri-stated. When set to 0, the MOSI pin will have an active output. Tri-state will allow some three-wire interfaces to work properly.

ECE External Clock Enable – This bit sets shift clock source.
0 = PHI2 and 1 = external Shift clock pin (14).

CPOL Clock Polarity – This bit sets the shift clock polarity.
0 = Rising edge; 1 = Falling edge

CPHA Clock Phase – This bit sets the shift clock phase.
0 = leading edge; 1 = falling edge

SCLK Divisor

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	D5	D4	D3	D2	D1	D0

(read/write)

The SCLK Divisor register contains the 6-bit value used to divide the Shift Clock source. $00 = CLK / 2 through $3F = CLK / 128.

Slave Select

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0

(read/write)

The Slave Select Register is used to set the 8 slave select outputs (SS0 – SS7).

Chip Initialization

The default power on state is all register bits set to 0. This includes the data, status, control, divisor, and slave select registers. A low on the /RES pin will also set all control, divisor, and slave select register bits to 0.

SPI Operation

The following is a guideline for initiating SPI communications.

1. If interrupt-driven transmission is desired, ensure an IRQ handler is enabled for the SPI interface.
2. If the TC bit in the SPI Status register is 1, then read the SPI Data register to clear it.
3. Enable Interrupts if desired, and set the Clock mode bits by writing to the SPI Control register.
4. Write the clock divisor value to the SCLK Divisor register.
5. Enable the appropriate Slave Select line by writing the Slave Select register.
6. Write first data byte to SPI Data register.
7. The TC bit will be set in the SPI Status register when shifting is complete.
8. Read the SPI Data register to get the incoming byte. The TC flag will clear after byte is read.
9. Process the incoming byte as required.
10. If you have more data to send or receive, repeat steps 6-9
11. After the last byte is received, de-select the Slave device.

Note 1. For fast transmit without polling and without receiving data, you can perform step 6 repeatedly without doing steps 7-9 as long as the SCLK rate is fast enough to keep up. When finished, do step 8 and 11 to clear the controller for the next operation.

Note 2. For fast receive without polling or sending data, Set the FRX bit in the control register and do steps 1 – 5. Now, just read the SPI data port, store the value, and repeat until you are done. The controller will automatically send the last byte written after each read. When done, set the FRX bit to 0 and do steps 8 and 11 to clear the controller for the next operation.

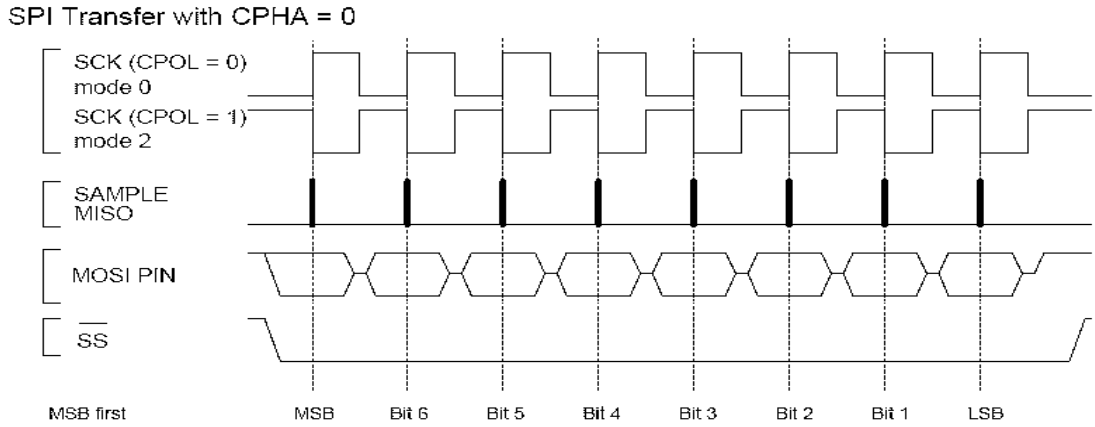
Note 3. For three wire interfaces, connect the MOSI and MISO pins together. Use the TMO bit in the control register to tri-state the MOSI pin during data reads, using the fast receive procedures in note 2.

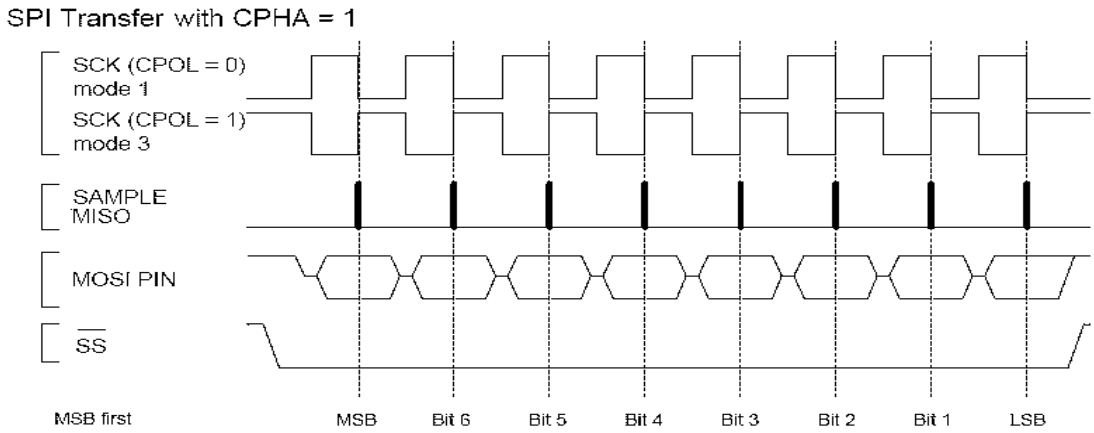
CPOL & CPHA Timing Reference

The following table describes how to configure the SPI modes:

SPI Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

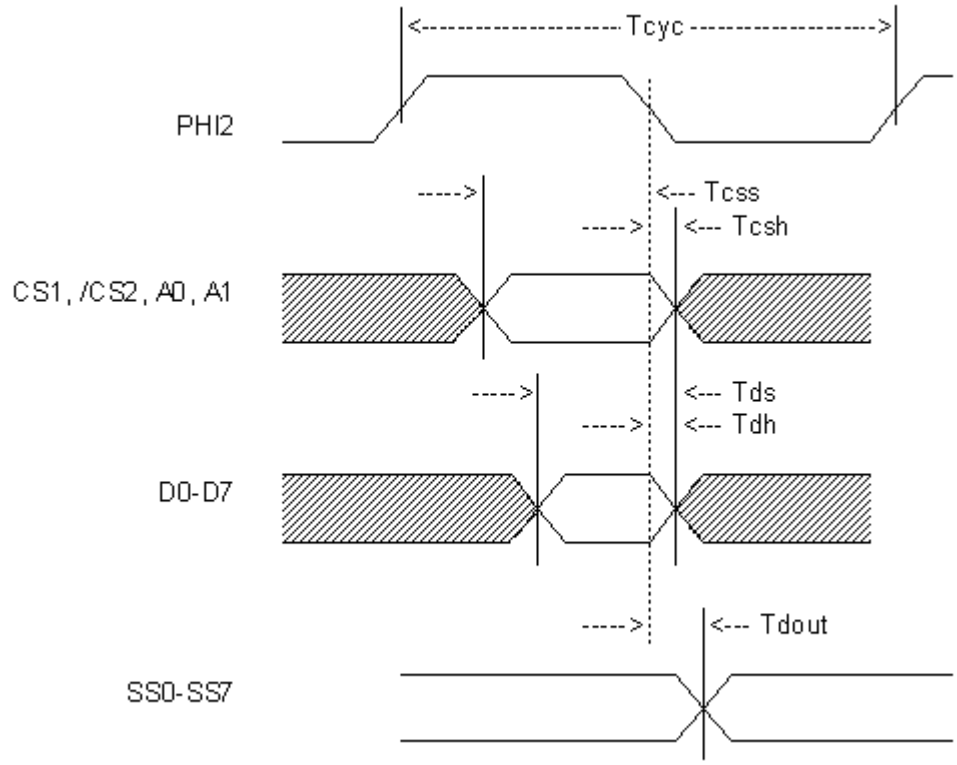
The following diagram details the relationship between CPOL, CPHA, SCLK, and the MISO/MOSI sampling:





Microprocessor Bus Timing

The following diagram details the timing relationships between PHI2, CS1, /CS2, A1, A0, & R/W, and SSx:



Symbol	Description	Min	Max	Unit
	PHI2 Frequency		14	MHz
Tcyc	PHI2 Cycle	71		ns
Tcss	Chip Select Setup	6		ns
Tcsh	Chip Select Hold	0.5		ns
Tds	Data setup	5		ns
Tdh	Data hold	0.5		ns
Tdout	Data out delay		15	ns
EXTC	External Clock		45	MHz

Revision History

Rev 1 – First release	June 8, 2008
Rev 2 – Removed ENA and replaced with TDR, Transmit Data Repeat.	June 13, 2008
Rev 3 – Removed TDR and replaced with TMO, Tri-state MOSI pin. Defined EXTC max frequency	June 29, 2008